

	L #	Hits	Search Text	DBs
1	L1	19226	(instruction prefetch\$3 fetch\$3) near10 (buffer queue)	USPAT; US-PGPUB
2	L2	53755	(combin\$3 complex) near5 (operation instruction)	USPAT; US-PGPUB
3	L4	6994	(instruction prefetch\$3 fetch\$3) near10 (buffer queue)	EPO; JPO; DERWENT; IBM_TDB
4	L5	11748	(combin\$3 complex) near5 (operation instruction)	EPO; JPO; DERWENT; IBM_TDB
5	L3	201	1 near30 2	USPAT; US-PGPUB
6	L6	16	4 near50 5	EPO; JPO; DERWENT; IBM_TDB
7	L9	202	1 near99 2	USPAT; US-PGPUB
8	L10	16	4 near99 5	EPO; JPO; DERWENT; IBM_TDB

	Docum ent ID	U	Title	Current OR
1	US 20040 04966 3 A1	<input type="checkbox"/>	System with wide operand architecture and method	712/222
2	US 20040 03467 8 A1	<input checked="" type="checkbox"/>	Efficient circuits for out-of-order microprocessors	708/446
3	US 20040 01975 3 A1	<input checked="" type="checkbox"/>	System and method for multiple store buffer forwarding in a system with a restrictive memory model	711/154
4	US 20030 10097 6 A1	<input checked="" type="checkbox"/>	Vehicle-mounted display system	701/1
5	US 20030 07911 3 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/205
6	US 20030 07006 0 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
7	US 20030 05608 7 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
8	US 20030 05608 6 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
9	US 20030 04651 9 A1	<input checked="" type="checkbox"/>	Progressive instruction folding in a processor with fast instruction decode	712/226
10	US 20030 00717 1 A1	<input checked="" type="checkbox"/>	Document production management in a distributed environment	358/1.1 5
11	US 20030 00526 5 A1	<input checked="" type="checkbox"/>	Checkpointing a superscalar, out-of-order processor for error recovery	712/218
12	US 20020 19906 7 A1	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
13	US 20020 19445 8 A1	<input checked="" type="checkbox"/>	VIRTUAL CONDITION CODES	712/227
14	US 20020 18446 0 A1	<input checked="" type="checkbox"/>	METHODS AND APPARATUS FOR COMBINING A PLURALITY OF MEMORY ACCESS TRANSACTIONS	711/167
15	US 20020 16994 4 A1	<input checked="" type="checkbox"/>	Method for prioritizing operations within a pipelined microprocessor based upon required results	712/204
16	US 20020 16198 9 A1	<input checked="" type="checkbox"/>	Apparatus and method for storing instruction set information	712/227
17	US 20020 15170 7 A1	<input checked="" type="checkbox"/>	Immune mediators and related methods	536/23. 5

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18	US 20020 14281 6 A1	<input checked="" type="checkbox"/>	Wagering system	463/6
19	US 20020 13368 2 A1	<input checked="" type="checkbox"/>	System with wide operand architecture, and method	711/165
20	US 20020 12081 3 A1	<input checked="" type="checkbox"/>	System and method for multiple store buffer forwarding in a system with a restrictive memory model	711/118
21	US 20020 10220 8 A1	<input checked="" type="checkbox"/>	RADIOLABELING KIT AND BINDING ASSAY	424/1.5 3
22	US 20020 09992 7 A1	<input checked="" type="checkbox"/>	System and method for determining operand access to data	712/216
23	US 20020 09191 4 A1	<input checked="" type="checkbox"/>	Multi-threading techniques for a processor utilizing a replay queue	712/219
24	US 20020 08779 3 A1	<input checked="" type="checkbox"/>	System and method for instruction cache re-ordering	711/125
25	US 20020 08770 9 A1	<input checked="" type="checkbox"/>	Stream processing node	709/231
26	US 20020 08557 4 A1	<input checked="" type="checkbox"/>	Stream switch fabric	370/412
27	US 20020 08241 1 A1	<input checked="" type="checkbox"/>	Immune mediators and related methods	536/23. 5
28	US 20020 02932 8 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
29	US 20020 01690 3 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
30	US 20010 04491 2 A1	<input checked="" type="checkbox"/>	Reliable hardware support for the use of formal languages in high assurance systems	714/30
31	US 66912 20 B1	<input checked="" type="checkbox"/>	Multiprocessor speculation mechanism via a barrier speculation flag	712/30
32	US 66843 23 B2	<input checked="" type="checkbox"/>	Virtual condition codes	712/226
33	US 66788 07 B2	<input checked="" type="checkbox"/>	System and method for multiple store buffer forwarding in a system with a restrictive memory model	711/154
34	US 66752 98 B1	<input checked="" type="checkbox"/>	Execution of instructions using op code lengths longer than standard op code lengths to encode data	713/190
35	US 66717 94 B1	<input checked="" type="checkbox"/>	Address generation interlock detection	712/217
36	US 66657 96 B1	<input checked="" type="checkbox"/>	Microprocessor instruction result obfuscation	713/190

	Docum ent ID	U	Title	Current OR
37	US 66657 92 B1	<input checked="" type="checkbox"/>	Interface to a memory system for a processor having a replay system	712/219
38	US 66530 84 B1	<input checked="" type="checkbox"/>	Anti-erbB-2 antibodies to human receptor related to but distinct from EGF receptor	435/7.1
39	US 66474 89 B1	<input checked="" type="checkbox"/>	Compare branch instruction pairing within a single integer pipeline	712/226
40	US 66474 85 B2	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
41	US 66437 65 B1	<input checked="" type="checkbox"/>	Programmable processor with group floating point operations	712/32
42	US 66292 71 B1	<input checked="" type="checkbox"/>	Technique for synchronizing faults in a processor having a replay system	714/49
43	US 66292 33 B1	<input checked="" type="checkbox"/>	Secondary reorder buffer microprocessor	712/218
44	US 66256 60 B1	<input checked="" type="checkbox"/>	Multiprocessor speculation mechanism for efficiently managing multiple barrier operations	709/248
45	US 66119 00 B2	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
46	US 66092 01 B1	<input checked="" type="checkbox"/>	Secure program execution using instruction buffer interdependencies	713/187
47	US 66091 94 B1	<input checked="" type="checkbox"/>	Apparatus for performing branch target address calculation based on branch type	712/238
48	US 66091 92 B1	<input checked="" type="checkbox"/>	System and method for asynchronously overlapping storage barrier operations with old and new storage operations	712/216
49	US 66091 89 B1	<input checked="" type="checkbox"/>	Cycle segmented prefix circuits	712/23
50	US 66067 02 B1	<input checked="" type="checkbox"/>	Multiprocessor speculation mechanism with imprecise recycling of storage operations	712/218
51	US 65981 66 B1	<input checked="" type="checkbox"/>	Microprocessor in which logic changes during execution	713/190
52	US 65980 63 B1	<input checked="" type="checkbox"/>	Fast calculation of (A/B)K by a parallel floating-point processor	708/606
53	US 65713 19 B2	<input checked="" type="checkbox"/>	Methods and apparatus for combining a plurality of memory access transactions	711/140
54	US 65464 62 B1	<input checked="" type="checkbox"/>	CLFLUSH micro-architectural implementation method and system	711/135
55	US 65429 86 B1	<input checked="" type="checkbox"/>	Resolving dependencies among concurrently dispatched instructions in a superscalar microprocessor	712/217
56	US 65196 83 B2	<input checked="" type="checkbox"/>	System and method for instruction cache re-ordering	711/125
57	US 65164 08 B1	<input checked="" type="checkbox"/>	Various length software breakpoint in a delay slot	712/227
58	US 64991 00 B1	<input checked="" type="checkbox"/>	Enhanced instruction decoding	712/210
59	US 64990 98 B1	<input checked="" type="checkbox"/>	Processor with instruction qualifiers to control MMU operation	712/209

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60	US 64347 42 B1	<input checked="" type="checkbox"/>	Symbol for automatically renaming symbols in files during the compiling of the files	717/140
61	US 64077 42 B1	<input checked="" type="checkbox"/>	Method and apparatus for combining multiple line elements to produce resultant line data	345/558
62	US 64053 03 B1	<input checked="" type="checkbox"/>	Massively parallel decoding and execution of variable-length instructions	712/210
63	US 63857 15 B1	<input checked="" type="checkbox"/>	Multi-threading for a processor utilizing a replay queue	712/219
64	US 63780 62 B1	<input checked="" type="checkbox"/>	Method and apparatus for performing a store operation	712/208
65	US 63539 24 B1	<input checked="" type="checkbox"/>	Method for back tracing program execution	717/128
66	US 63493 83 B1	<input checked="" type="checkbox"/>	System for combining adjacent push/pop stack program instructions into single double push/pop stack microinstruction for execution	712/226
67	US 63470 55 B1	<input checked="" type="checkbox"/>	Line buffer type semiconductor memory device capable of direct prefetch and restore operations	365/189 .05
68	US 63381 36 B1	<input checked="" type="checkbox"/>	Pairing of load-ALU-store with conditional branch	712/221
69	US 63306 57 B1	<input checked="" type="checkbox"/>	Pairing of micro instructions in the instruction queue	712/23
70	US 63213 03 B1	<input checked="" type="checkbox"/>	Dynamically modifying queued transactions in a cache memory system	711/140
71	US 63112 54 B1	<input checked="" type="checkbox"/>	Multiple store miss handling in a cache memory memory system	711/126
72	US 63049 53 B1	<input checked="" type="checkbox"/>	Computer processor with instruction-specific schedulers	712/215
73	US 63016 51 B1	<input checked="" type="checkbox"/>	Method and apparatus for folding a plurality of instructions	712/202
74	US 62955 99 B1	<input checked="" type="checkbox"/>	System and method for providing a wide operand architecture	712/32
75	US 62826 30 B1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
76	US 62726 19 B1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
77	US 62694 27 B1	<input checked="" type="checkbox"/>	Multiple load miss handling in a cache memory system	711/140
78	US 62567 20 B1	<input checked="" type="checkbox"/>	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
79	US 62405 08 B1	<input checked="" type="checkbox"/>	Decode and execution synchronized pipeline processing using decode generated memory read queue with stop entry to allow execution generated memory read	712/219
80	US 62329 74 B1	<input checked="" type="checkbox"/>	Decision-theoretic regulation for allocating computational resources among components of multimedia content to improve fidelity	345/419
81	US 62232 58 B1	<input checked="" type="checkbox"/>	Method and apparatus for implementing non-temporal loads	711/138
82	US 62232 54 B1	<input checked="" type="checkbox"/>	Parcel cache	711/125

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83	US 62090 82 B1	<input checked="" type="checkbox"/>	Apparatus and method for optimizing execution of push all/pop all instructions	712/225
84	US 62055 20 B1	<input checked="" type="checkbox"/>	Method and apparatus for implementing non-temporal stores	711/138
85	US 61890 87 B1	<input checked="" type="checkbox"/>	Superscalar instruction decoder including an instruction queue	712/208
86	US 61848 91 B1	<input checked="" type="checkbox"/>	Fog simulation for partially transparent objects	345/426
87	US 61700 53 B1	<input checked="" type="checkbox"/>	Microprocessor with circuits, systems and methods for responding to branch instructions based on history of prediction accuracy	712/240
88	US 61287 23 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
89	US 61192 20 A	<input checked="" type="checkbox"/>	Method of and apparatus for supplying multiple instruction strings whose addresses are discontinued by branch instructions	712/235
90	US 61015 94 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
91	US 60981 65 A	<input checked="" type="checkbox"/>	Fetching and handling a bundle of instructions comprising instructions and non-complex instructions	712/215
92	US 60921 81 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/206
93	US 60789 93 A	<input checked="" type="checkbox"/>	Data supplying apparatus for independently performing hit determination and data access	711/128
94	US 60761 45 A	<input checked="" type="checkbox"/>	Data supplying apparatus for independently performing hit determination and data access	711/125
95	US 60732 10 A	<input checked="" type="checkbox"/>	Synchronization of weakly ordered write combining operations using a fencing mechanism	711/118
96	US 60643 93 A	<input checked="" type="checkbox"/>	Method for measuring the fidelity of warped image layer approximations in a real-time graphics rendering pipeline	345/427
97	US 60617 72 A	<input checked="" type="checkbox"/>	Split write data processing mechanism for memory controllers utilizing inactive periods during write data processing for other transactions	711/169
98	US 60527 76 A	<input checked="" type="checkbox"/>	Branch operation system where instructions are queued until preparations is ascertained to be completed and branch distance is considered as an execution condition	712/233
99	US 60444 50 A	<input checked="" type="checkbox"/>	Processor for VLIW instruction	712/24
100	US 60386 54 A	<input checked="" type="checkbox"/>	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
101	US 60386 53 A	<input checked="" type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
102	US 60353 94 A	<input checked="" type="checkbox"/>	System for providing high performance speculative processing of complex load/store instructions by generating primitive instructions in the load/store unit and sequencer in parallel	712/245
103	US 60161 50 A	<input checked="" type="checkbox"/>	Sprite compositor and method for performing lighting and shading operations using a compositor to combine factored image layers	345/426
104	US 60063 18 A	<input checked="" type="checkbox"/>	General purpose, dynamic partitioning, programmable media processor	712/28
105	US 59855 53 A	<input checked="" type="checkbox"/>	erbB-2 gene segments, probes, recombinant DNA and kits for detection	435/6

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106	US 59616 29 A	<input checked="" type="checkbox"/>	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
107	US 59419 83 A	<input checked="" type="checkbox"/>	Out-of-order execution using encoded dependencies between instructions in queues to determine stall values that control issuance of instructions from the queues	712/214
108	US 59238 71 A	<input checked="" type="checkbox"/>	Multifunctional execution unit having independently operable adder and multiplier	712/221
109	US 58965 18 A	<input checked="" type="checkbox"/>	Instruction queue scanning using opcode identification	712/208
110	US 58872 43 A	<input checked="" type="checkbox"/>	Signal processing apparatus and methods	725/136
111	US 58840 69 A	<input checked="" type="checkbox"/>	Computer and a method of operating a computer to combine data values within a singularly addressable data string	712/221
112	US 58812 65 A	<input checked="" type="checkbox"/>	Computer processor with distributed pipeline control that allows functional units to complete operations out of order while maintaining precise interrupts	712/218
113	US 58753 26 A	<input checked="" type="checkbox"/>	Data processing system and method for completing out-of-order instructions	712/244
114	US 58753 16 A	<input checked="" type="checkbox"/>	Method for handling complex instructions in an out-of-order processor	712/215
115	US 58322 92 A	<input checked="" type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
116	US 58226 03 A	<input checked="" type="checkbox"/>	High bandwidth media processor interface for transmitting data in the form of packets with requests linked to associated responses by identification data	712/1
117	US 58225 56 A	<input checked="" type="checkbox"/>	Distributed completion control in a microprocessor	712/205
118	US 58093 21 A	<input checked="" type="checkbox"/>	General purpose, multiple precision parallel operation, programmable media processor	712/1
119	US 58093 20 A	<input checked="" type="checkbox"/>	High-performance multi-processor having floating point unit	712/34
120	US 58058 49 A	<input checked="" type="checkbox"/>	Data processing system and method for using an unique identifier to maintain an age relationship between executing instructions	712/214
121	US 57969 73 A	<input checked="" type="checkbox"/>	Method and apparatus for decoding one or more complex instructions into concurrently dispatched simple instructions	712/208
122	US 57940 61 A	<input checked="" type="checkbox"/>	General purpose, multiple precision parallel operation, programmable media processor	712/1
123	US 57940 60 A	<input checked="" type="checkbox"/>	General purpose, multiple precision parallel operation, programmable media processor	712/1
124	US 57747 12 A	<input checked="" type="checkbox"/>	Instruction dispatch unit and method for mapping a sending order of operations to a receiving order	712/245
125	US 57713 66 A	<input checked="" type="checkbox"/>	Method and system for interchanging operands during complex instruction execution in a data processing system	712/217
126	US 57652 20 A	<input checked="" type="checkbox"/>	Apparatus and method to reduce instruction address storage in a super-scaler processor	711/220
127	US 57581 16 A	<input checked="" type="checkbox"/>	Instruction length decoder for generating output length indicia to identify boundaries between variable length instructions	712/210
128	US 57519 96 A	<input checked="" type="checkbox"/>	Method and apparatus for processing memory-type information within a microprocessor	711/145

	Docum ent ID	U	Title	Current OR
129	US 57489 76 A	<input checked="" type="checkbox"/>	Mechanism for maintaining data coherency in a branch history instruction cache	712/240
130	US 57472 61 A	<input checked="" type="checkbox"/>	Protein related to but distinct from EGF receptor and antibodies reactive therewith	435/7.1
131	US 57428 40 A	<input checked="" type="checkbox"/>	General purpose, multiple precision parallel operation, programmable media processor	712/210
132	US 57064 66 A	<input checked="" type="checkbox"/>	Von Neumann system with harvard processor and instruction buffer	711/125
133	US 56937 78 A	<input checked="" type="checkbox"/>	Arg a human gene related to but distinct from abl proto-oncogene	536/23.5
134	US 56897 20 A	<input checked="" type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution	712/23
135	US 56824 92 A	<input checked="" type="checkbox"/>	Computer processor with distributed pipeline control that allows functional units to complete operations out of order while maintaining precise interrupts	712/214
136	US 56757 29 A	<input checked="" type="checkbox"/>	Method and apparatus for performing on-chip measurement on a component	714/37
137	US 56642 15 A	<input checked="" type="checkbox"/>	Data processor with an execution unit for performing load instructions and method of operation	712/23
138	US 56550 96 A	<input checked="" type="checkbox"/>	Method and apparatus for dynamic scheduling of instructions to ensure sequentially coherent data in a processor employing out-of-order execution	712/200
139	US 56300 82 A	<input checked="" type="checkbox"/>	Apparatus and method for instruction queue scanning	712/213
140	US 56300 75 A	<input checked="" type="checkbox"/>	Write combining buffer for sequentially addressed partial line operations originating from a single instruction	711/100
141	US 56257 88 A	<input checked="" type="checkbox"/>	Microprocessor with novel instruction for signaling event occurrence and for providing event handling information in response thereto	712/214
142	US 55985 46 A	<input checked="" type="checkbox"/>	Dual-architecture super-scalar pipeline	712/209
143	US 55985 44 A	<input checked="" type="checkbox"/>	Instruction buffer device for processing an instruction set of variable-length instruction codes	712/204
144	US 55926 34 A	<input checked="" type="checkbox"/>	Zero-cycle multi-state branch cache prediction data processing system and method thereof	712/239
145	US 55862 95 A	<input checked="" type="checkbox"/>	Combination prefetch buffer and instruction cache	711/137
146	US 55617 80 A	<input checked="" type="checkbox"/>	Method and apparatus for combining uncacheable write data into cache-line-sized write buffers	711/126
147	US 55600 32 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
148	US 55420 58 A	<input checked="" type="checkbox"/>	Pipelined computer with operand context queue to simplify context-dependent execution flow	713/502
149	US 55399 11 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
150	US 55264 98 A	<input checked="" type="checkbox"/>	Pipeline processor, with a return address stack and two stack pointers, for storing pre-return processed addresses	712/239
151	US 55009 43 A	<input checked="" type="checkbox"/>	Data processor with rename buffer and FIFO buffer for in-order instruction completion	712/218

	Docum ent ID	U	Title	Current OR
152	US 54887 30 A	<input checked="" type="checkbox"/>	Register conflict scoreboard in pipelined computer using pipelined reference counts	712/41
153	US 54816 89 A	<input checked="" type="checkbox"/>	Conversion of internal processor register commands to I/O space addresses	711/202
154	US 54816 85 A	<input checked="" type="checkbox"/>	RISC microprocessor architecture implementing fast trap and exception state	712/244
155	US 54715 91 A	<input checked="" type="checkbox"/>	Combined write-operand queue and read-after-write dependency scoreboard	712/217
156	US 54505 55 A	<input checked="" type="checkbox"/>	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228
157	US 54487 05 A	<input checked="" type="checkbox"/>	RISC microprocessor architecture implementing fast trap and exception state	712/244
158	US 54427 57 A	<input checked="" type="checkbox"/>	Computer processor with distributed pipeline control that allows functional units to complete operations out of order while maintaining precise interrupts	712/218
159	US 54386 68 A	<input checked="" type="checkbox"/>	System and method for extraction, alignment and decoding of CISC instructions into a nano-instruction bucket for execution by a RISC computer	712/204
160	US 54370 21 A	<input checked="" type="checkbox"/>	Programmable dedicated timer operating on a clock independent of processor timer	713/502
161	US 53945 29 A	<input checked="" type="checkbox"/>	Branch prediction unit for high-performance processor	712/240
162	US 53718 60 A	<input checked="" type="checkbox"/>	Programmable controller	710/22
163	US 53613 37 A	<input checked="" type="checkbox"/>	Method and apparatus for rapidly switching processes in a computer system	712/228
164	US 53554 59 A	<input checked="" type="checkbox"/>	Pipeline processor, with return address stack storing only pre-return processed addresses for judging validity and correction of unprocessed address	712/242
165	US 53352 77 A	<input checked="" type="checkbox"/>	Signal processing apparatus and methods	380/242
166	US 53332 97 A	<input checked="" type="checkbox"/>	Multiprocessor system having multiple classes of instructions for purposes of mutual interruptibility	710/200
167	US 53332 96 A	<input checked="" type="checkbox"/>	Combined queue for invalidates and return data in multiprocessor system	711/171
168	US 53177 20 A	<input checked="" type="checkbox"/>	Processor system with writeback cache using writeback and non writeback transactions stored in separate queues	711/143
169	US 53177 01 A	<input checked="" type="checkbox"/>	Method for refilling instruction queue by reading predetermined number of instruction words comprising one or more instructions and determining the actual number of instruction words used	712/207
170	US 53136 02 A	<input checked="" type="checkbox"/>	Multiprocessor system and method of control over order of transfer of data between buffer storages	711/100
171	US 52336 54 A	<input checked="" type="checkbox"/>	Signal processing apparatus and methods	725/135
172	US 52261 26 A	<input checked="" type="checkbox"/>	Processor having plurality of functional units for orderly retiring outstanding operations based upon its associated tags	712/218
173	US 51971 45 A	<input checked="" type="checkbox"/>	Buffer storage system using parallel buffer storage units and move-out buffer registers	711/143

	Docum ent ID	U	Title	Current OR
174	US 51932 05 A	<input checked="" type="checkbox"/>	Pipeline processor, with return address stack storing only pre-return processed address for judging validity and correction of unprocessed address	712/239
175	US 51670 26 A	<input checked="" type="checkbox"/>	Simultaneously or sequentially decoding multiple specifiers of a variable length pipeline instruction based on detection of modified value of specifier registers	712/210
176	US 51631 39 A	<input checked="" type="checkbox"/>	Instruction preprocessor for conditionally combining short memory instructions into virtual long instructions	712/206
177	US 51558 43 A	<input checked="" type="checkbox"/>	Error transition mode for multi-processor system	714/5
178	US 51485 28 A	<input checked="" type="checkbox"/>	Method and apparatus for simultaneously decoding three operands in a variable length instruction when one of the operands is also of variable length	712/210
179	US 51426 34 A	<input checked="" type="checkbox"/>	Branch prediction	712/240
180	US 51426 33 A	<input checked="" type="checkbox"/>	Preprocessing implied specifiers in a pipelined processor	712/225
181	US 51426 31 A	<input checked="" type="checkbox"/>	System for queuing individual read or write mask and generating respective composite mask for controlling access to general purpose register	712/217
182	US 51310 86 A	<input checked="" type="checkbox"/>	Method and system for executing pipelined three operand construct	712/213
183	US 51094 14 A	<input checked="" type="checkbox"/>	Signal processing apparatus and methods	725/135
184	US 51013 41 A	<input checked="" type="checkbox"/>	Pipelined system for reducing instruction access time by accumulating predecoded instruction bits a FIFO	712/213
185	US 49929 32 A	<input checked="" type="checkbox"/>	Data processing device with data buffer control	712/237
186	US 49658 25 A	<input checked="" type="checkbox"/>	Signal processing apparatus and methods	380/233
187	US 49106 57 A	<input checked="" type="checkbox"/>	Microprocessor providing bus access for unconditional instruction execution	712/207
188	US 49013 60 A	<input checked="" type="checkbox"/>	Gated architecture for computer vision machine	382/303
189	US 48093 47 A	<input checked="" type="checkbox"/>	Computer vision architecture	382/240
190	US 48093 46 A	<input checked="" type="checkbox"/>	Computer vision architecture for iconic to symbolic transformation	382/302
191	US 47759 27 A	<input checked="" type="checkbox"/>	Processor including fetch operation for branch instruction with control tag	712/207
192	US 47617 31 A	<input checked="" type="checkbox"/>	Look-ahead instruction fetch control for a cache memory	711/156
193	US 46987 47 A	<input checked="" type="checkbox"/>	Instruction address calculation unit for a microprocessor	712/42
194	US 46033 30 A	<input checked="" type="checkbox"/>	Font display and text editing system with character overlay feature	345/467
195	US 45846 44 A	<input checked="" type="checkbox"/>	Method of controlling use of resources in a data processing system by at least two processes	710/260
196	US 45817 02 A	<input checked="" type="checkbox"/>	Critical system protection	711/207

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197	US 45743 48 A	<input checked="" type="checkbox"/>	High speed digital signal processor architecture	712/215
198	US 37876 73 A	<input checked="" type="checkbox"/>	PIPELINED HIGH SPEED ARITHMETIC UNIT	708/521
199	US 36752 09 A	<input checked="" type="checkbox"/>	AUTONOMOUS MULTIPLE-PATH INPUT/OUTPUT CONTROL SYSTEM	710/5
200	US 36147 42 A	<input checked="" type="checkbox"/>	AUTOMATIC CONTEXT SWITCHING IN A MULTIPROGRAMMED MULTIPROCESSOR SYSTEM	718/108

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1	JP 06059 934 A	<input type="checkbox"/>	PROGRAM EVALUATING MICROCOMPUTER	
2	JP 01306 932 A	<input checked="" type="checkbox"/>	METHOD FOR TESTING DATA PROCESSOR	
3	JP 60020 256 A	<input checked="" type="checkbox"/>	CONTROL SYSTEM OF BUFFER STORAGE DEVICE	
4	EP 72421 4 A2	<input checked="" type="checkbox"/>	Distributed completion control in a microprocessor	
5	EP 69765 0 A2	<input checked="" type="checkbox"/>	Apparatus and method for instruction queue scanning.	
6	EP 65132 0 A1	<input checked="" type="checkbox"/>	Superscalar instruction decoder.	
7	WO 90030 01 A1	<input checked="" type="checkbox"/>	PIPELINE STRUCTURES AND METHODS	
8	US 20020 08783 6 A	<input checked="" type="checkbox"/>	Microprocessor for complex instruction set computer architecture, has physical registers that are reclaimed from old field of active list to free list, whenever dispatched instructions retire from instruction buffer window	
9	US 63306 57 B	<input checked="" type="checkbox"/>	Micro instruction pairing apparatus for use with pipeline microprocessor combines ordered micro instructions that are obtained from micro instruction queue, so that micro instructions are executed in parallel	
10	US 60732 10 A	<input checked="" type="checkbox"/>	Weakly ordered write combining operation synchronization method for microprocessor system, involves blocking store fence instruction, if a weakly ordered write combining operation already exists in buffer	
11	EP 99288 7 A	<input checked="" type="checkbox"/>	Digital system comprising microprocessor used in mobile telecommunications applications has instruction buffer unit that decodes second instruction from instructions sequence in combined manner while decoding first instruction	
12	JP 11073 318 A	<input checked="" type="checkbox"/>	Microprocessor for combined execution of instructions - has address generating unit that outputs write-in or reading address of instruction buffer based on control signal received from instruction issue unit or instruction decoder, respectively	
13	EP 91853 6 B	<input checked="" type="checkbox"/>	Compositions for treatment of hyperglycaemic disorders such as diabetes - comprise insulin-like growth factor-1 and neutral protamine hagedorn insulin	
14	US 57428 40 A	<input checked="" type="checkbox"/>	Execution unit which maintains peak data throughput in unified extension of multiple media data streams - has extended mathematical element coupled to data path and programmable to implement additional mathematical operations at peak data throughput	
15	EP 43634 1 A	<input checked="" type="checkbox"/>	Pre-fetch sequencer for retrieving instructions for computer memory - using instruction words and queue to move words from instruction pipeline	
16	US 51013 41 A	<input checked="" type="checkbox"/>	Early decoding methods for pipeline structures - stores pre-decoded instruction bits in buffer before executing in operand execute pipeline	